REMARKS

Claims 1-7, 15-26, and 30-34 are pending. Claims 1, 15, and 19 are in independent form.

CLAIM 1: In the action mailed August 8, claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,933,627 to Parady (hereinafter "Parady") and U.S. Patent No. 5,875,470 to Dreibelbis et al. (hereinafter "Dreibelbis").

Claim 1 relates to an execution unit for execution of multiple context threads. The execution unit comprises an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the arithmetic logic unit. The register set includes a plurality of two-ported random access memory devices assembled into banks. The register set includes two effective read ports and one effective write port. Each bank is capable of performing a read and a write to two different words in the same processor cycle. The arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port.

The rejection contends that it would have been obvious for one of ordinary skill to have combined Parady and Dreibelbis to have arrived at the subject matter of claim 1. Applicant respectfully disagrees.

For example, Parady and Dreibelbis neither describe nor suggest a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port. In this regard, Paraday is silent as to the architecture of integer registers 48. Indeed, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1. Certainly nothing about Parady's registers describes or suggests that integer registers 48 comprise a plurality of two-ported random access memory devices.

The only mention of two-ported register files made in Parady is found at col. 5, line 30-43. In this section, Parady acknowledges that multi-ported register files can occupy more silicon than simple duplication of registers. However, the duplication of dual ported register files described by Parady does not suggest a register set that comprises a plurality of two-ported random access memory devices and that includes two effective read ports and one effective write port. For example, FIG. 7 illustrates how Parady envisages dual ported register files can be duplicated. In particular, dual ported shadow registers 186 are to be individually addressed using a data switch 192 or individually enabled for writing along a path 194.

Such individual addressing or individual enablement does not provide a register set that comprises two-ported random access memory devices and includes two effective read ports and one effective write port, as recited in claim 1. Rather, individual addressing or individual enablement of a dual ported register file inherently limits the effective ports to two—i.e., the two ports on the individually addressed or individually enabled dual ported register file.

Dreibelbis does nothing to remedy this deficiency in Parady. In this regard, Dreibelbis describes that multiple DRAM banks can be packaged on a single chip and accessed using multiple bidirectional ports. *See, e.g., Driebelbis*, col. 1, line 40-41. Driebelbis's DRAM banks are not assembled from two-ported random access memory devices, as recited in claim 1. Moreover, given that each port is bidirectional, the contention that Dreibelbis' register set somehow includes two effective read ports and one effective write port is without basis. Applicant is at a loss to understand why one of ordinary skill would consider a bidirectional port to be two effective read ports and one effective write port. Dreibelbis thus also fails to describe or suggest a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port.

Accordingly, claim 1 is not obvious over Paraday and Dreibelbis. Applicant therefore respectfully requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

CLAIM 15: Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Dreibelbis.

Claim 15 relates to a method for executing multiple context threads. The method includes processing data for executing threads within an arithmetic logic unit, operating control logic to control the arithmetic logic unit, and storing and obtaining operands for the arithmetic logic unit within a general purpose register set comprising a plurality of banks of two-ported random access memory devices. The register set comprises two effective read ports and one effective write port. The effective write port includes a single write line to write to addresses in different banks of the plurality of banks. Each bank is capable of performing a read and a write to two different words in the same processor cycle.

The rejection contends that it would have been obvious for one of ordinary skill to have combined Parady and Dreibelbis to have arrived at the subject matter of claim 15. Applicant respectfully disagrees.

For example, Parady and Dreibelbis neither describe nor suggest a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port. In this regard, as discussed above, nothing about Parady's registers describes or suggests that integer registers 48 comprise a plurality of two-ported random access memory devices.

Dreibelbis does nothing to remedy this deficiency in Parady. Driebelbis's DRAM banks are not assembled from two-ported random access memory devices. Moreover, given that each port in Dreibelbis is bidirectional, the contention that Dreibelbis' register set somehow includes two effective read ports and one effective write port is without basis.

Accordingly, claim 15 is not obvious over Paraday and Dreibelbis. Applicant therefore respectfully requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

CLAIM 19: Claim 19 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Dreibelbis.

Claim 19 relates to a processor unit that includes an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, a general purpose register set to

store and obtain operands for the arithmetic logic unit, and a data link between the arithmetic logic unit and the one effective write port of the general purpose register set. The register set includes a plurality of two-ported random access memory devices. The register set includes two effective read ports and one effective write port. The data link allows the arithmetic logic unit to write to different two-ported random access memory devices in the general purpose register set through the one effective write port.

The rejection contends that it would have been obvious for one of ordinary skill to have combined Parady and Dreibelbis to have arrived at the subject matter of claim 19. Applicant respectfully disagrees.

For example, Parady and Dreibelbis neither describe nor suggest a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port. In this regard, as discussed above, nothing about Parady's registers describes or suggests that integer registers 48 comprise a plurality of two-ported random access memory devices.

Dreibelbis does nothing to remedy this deficiency in Parady. Driebelbis's DRAM banks are not assembled from two-ported random access memory devices. Moreover, given that each port in Dreibelbis is bidirectional, the contention that

Dreibelbis' register set somehow includes two effective read ports and one effective write port is without basis.

Accordingly, claim 19 is not obvious over Paraday and Dreibelbis. Applicant therefore respectfully requests that the rejections of claim 19 and the claims dependent therefrom be withdrawn.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. Please apply the Petition for One-Month Extension of Time and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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